**SE 3K04 Assignment 1**

**Part 3: Hardware Hiding**

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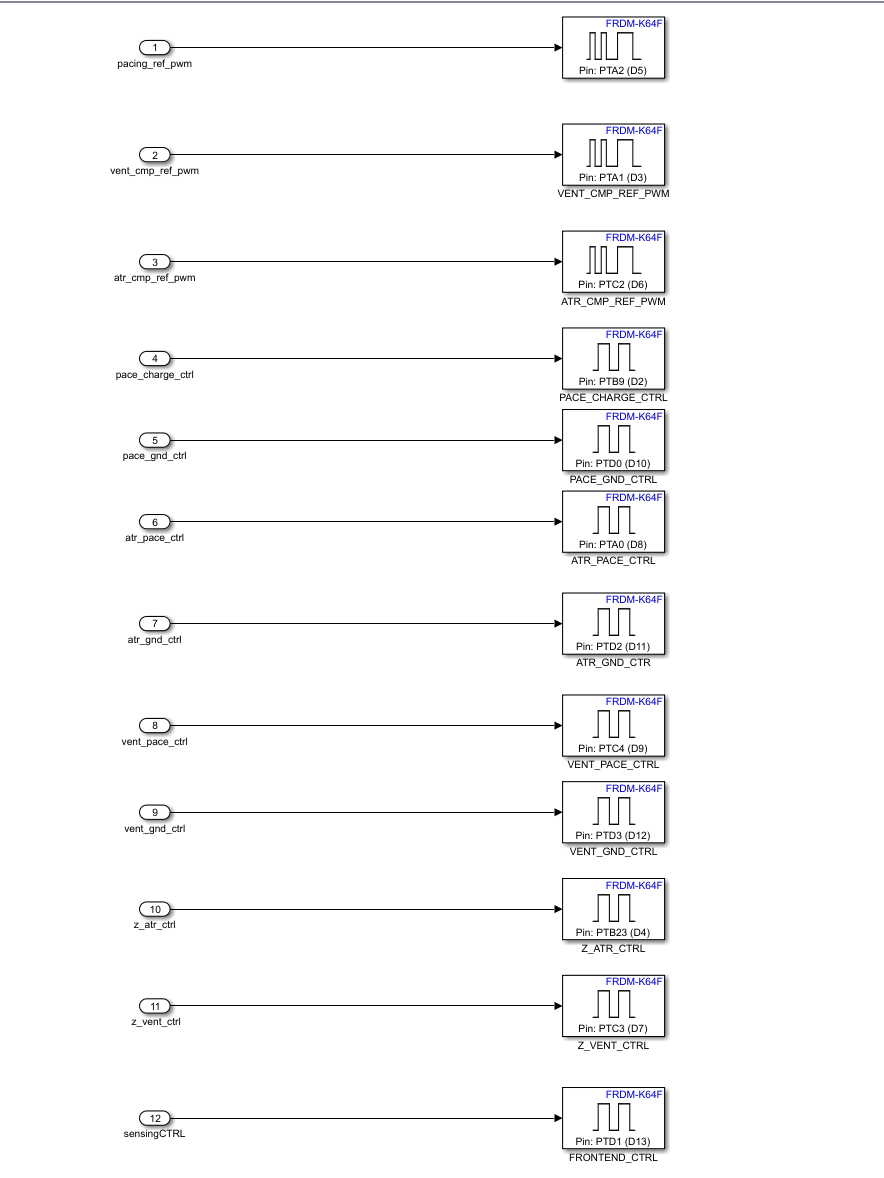
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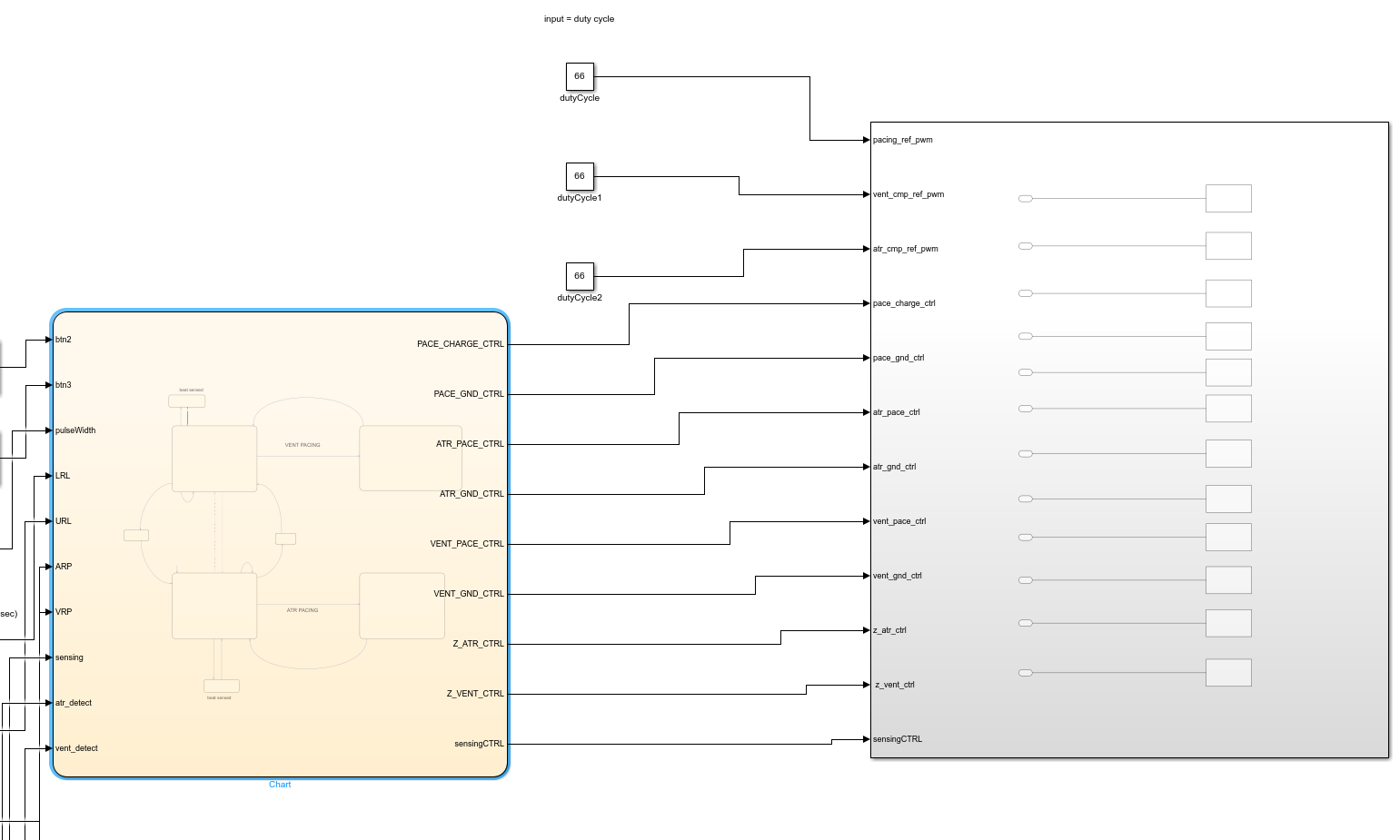
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## Design Decision

In order to achieve hardware hiding, Subsystem from Simulink is used to map the pin to the hardware model. The pins are mapped corresponding to the requirements which implements AOO,AAI,VOO,VVI. The hardware mapped is a FRDM K64F microcontroller.

## Detailed Description





|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Input to Subsystem | Min | Max | Current Value | DataType | Description |
| PACE\_CHARGE\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D2 in FRDM-L64F to start and stop charging of C22 capacitor |
| PACE\_GND\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D10 in FRDM-L64F for current flow in atrium and ventricle |
| ATR\_PACE\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D8 in FRDM-L64F for current flow to atrium when pacing |
| ATR\_GND\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D11 in FRDM-L64F for discharging capacitor c21 when pacing atrium |
| VENT\_GND\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D12 in FRDM-L64F for discharging capacitor c21 when pacing ventricle |
| Z\_ATR\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D4 in FRDM-L64F for analyzing atrial electrode impedance |
| Z\_VENT\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D4 in FRDM-L64F for analyzing ventricular electrode impedance |
| sensing\_CTRL | 0 | 1 | Control by states | boolean | Output to pin D13 in FRDM-L64F for Frontend\_CTRL specified for activate sensing circuitry |
| pacing\_ref\_pwm | 0 | 100 | 66% | double | Output to pin D5 for generating PWM voltage to chagrin capacitor C22 |
| pacing\_ref\_pwm | 0 | 100 | 66% | double | Output to pin D3 to establish threshold voltage for comparing with natural ventricular beat |
| atr\_cmp\_ref\_pwm | 0 | 100 | 66% | double | Output to pin D3 to establish threshold voltage for comparing with natural atrium beat |

## Requirements changes that are likely

* pacing\_ref\_pwm, pacing\_ref\_pwma and atr\_cmp\_ref\_pwm for modes AOO, VOO, AAI, VVI are needed to be changed to let users put input of duty cycles through DCM.

## Design Decisions that are likely

* The form of input of duty cycles will be changed to user input from DCM rather than constant module in simulink.

## Testing

|  |  |  |  |
| --- | --- | --- | --- |
| **Test Case** | **Mode Selected** | **Result (pass/fail)** | **Additional Description** |
| All mapping of the pin are correct regarding test case in part 1 document | AOO,AAI,VOO,VVI | pass | The test cases are included in part 1 document, all test cases passed. All pins are correct with the assignment |
| Duty cycles have the correct effect on PWM output | AOO,AAI,VOO,VVI | pass | PWM has the expected effect of the pacing amplitude. Tested through different input values. |
| Duty cycle have the correct effect on establishing threshold for sensing mode | AAI,VVI | pass | All the threshold values are established. Tested through differen tinput values. |